COL215 Hardware Assignment 2

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(2021CS10571 and 2021CS10134)

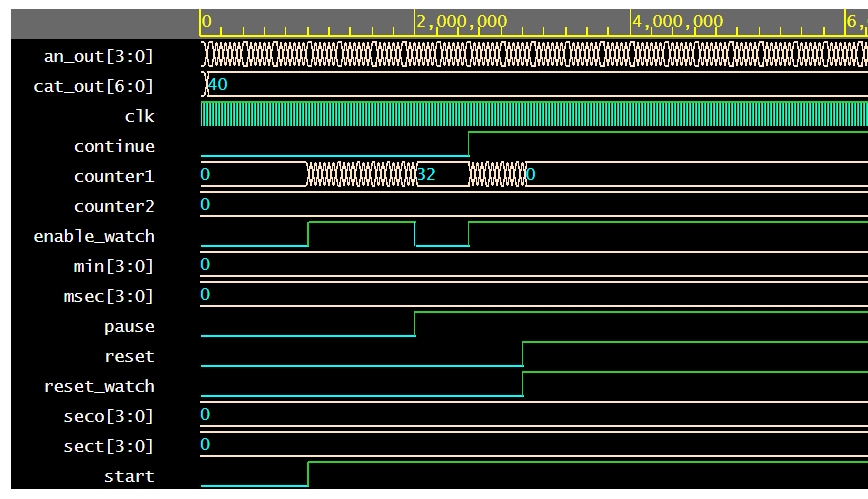
## Design Decisions and Lab Work

We added the decimal point in our timing module and used the combine module created in the last assignment. We made two counters, counter1 for incrementing after each clock period (10ns) and counter2 for incrementing whenever counter1 reaches 107. Counter2 represents the count for 10th second. Using counter2, we derive the values of minutes, tens of seconds, unit of seconds and tenths of seconds.

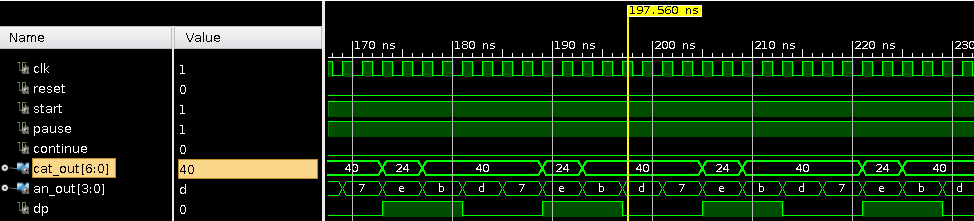
Then we made the logic for enable\_watch and reset\_watch using their truth tables, and controlled the counters using these two signals.

## Simulations

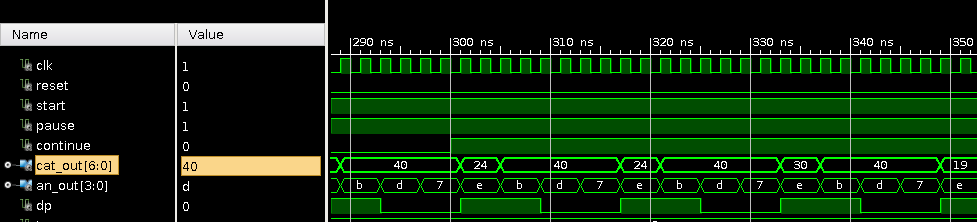
Showing working of start, pause, reset and continue



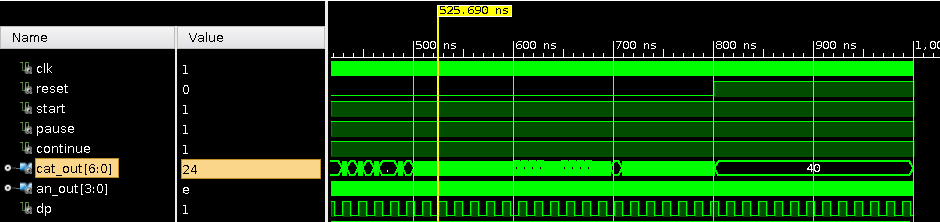
On pressing pause, the display gets stopped



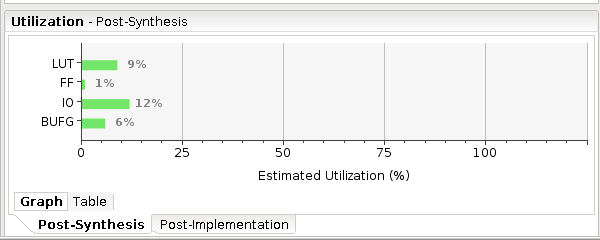
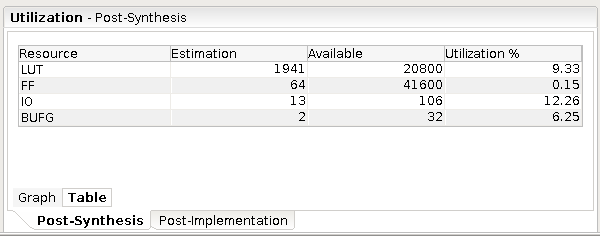
On continue, it starts again



After reset is ON, cat\_out goes to zero



## Synthesis Report

*Note: The Vivado Synthesis Report and Utilization Report have been added in the zip file as separate .txt files*

## Block Diagram

